AMENDMENTS TO THE DRAWINGS

Please delete FIG. 4.

REMARKS

I. Status of Application

By the present Amendment, claim 8 has been canceled without prejudice or disclaimer. Upon entry of the present Amendment, claims 1 and 3-7 are all the claims pending in the application. Claims 1 and 3-8 have been rejected.

II. Objections to the Specification

The Examiner has objected to the specification alleging that the amended specification on pages 5 and 6 and FIG. 4 introduces new matter into the disclosure. Further, the Examiner alleges that Applicant is required to cancel the new matter in the reply to the Office Action.

Applicant respectfully traverses these objections. Nevertheless, without conceding to the merits of the Examiner's objections, Applicant has amended the specification and drawings, as set forth above, to omit the portions that the Examiner deems objectionable. Accordingly, Applicant respectfully requests that the Examiner withdraw these objections.

III. Objections to the Drawings

The Examiner has objected to the drawings alleging that the drawings must show "a computer readable medium" as recited in claim 8, and its connection with the disclosed apparatus. Without conceding to the merits of the Examiner's objections, claim 8 has been canceled without prejudice or disclaimer and, therefore, the Examiner's objections to the drawings are now moot.

IV. Claim Rejections Under 35 U.S.C. § 112

Claim 8 is rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. Without conceding to the merits of the Examiner's rejection,

claim 8 has been canceled without prejudice or disclaimer and, therefore, the Examiner's rejection of claim 8 is now moot.

V. Claim Rejections Under 35 U.S.C. § 103

Claims 1 and 3-8 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Pathak et al. (7,158,727) in view of LaGasse et al. (2003/0020985). Applicant respectfully traverses these rejections.

As an initial matter, Applicant notes that claim 8 has been canceled without prejudice or disclaimer and, therefore, the Examiner's rejection of claim 8 is now moot.

Additionally, independent claim 1 recites (among other things):

> ...a frequency multiplicator unit, which frequency-multiplies the converted electrical data signal, thereby producing a frequency-multiplied signal; and
>
> a clock recovery unit comprising a phased locked loop circuit,
>
> wherein the frequency-multiplied signal is used to drive the phase locked loop circuit...

The Examiner was persuaded by arguments advanced with the Amendment filed on December 22, 2008 that the cited Pathak reference's teachings regarding electrical-to-optical converter / 4:1 multiplexer 108 do not correspond to a frequency multiplicator unit, as claimed. In response to such arguments, the Examiner sets forth new grounds of rejection relying on column 3, lines 7-16 of Pathak as allegedly teaching the features of "a frequency multiplicator unit," as recited in claim 1. The grounds of rejection also allege that Pathak's teachings regarding a clock/data recovery module 103 corresponds to "a clock recovery unit," as claimed. Applicant respectfully disagrees with the grounds of rejection.

First, column 3, lines 7-16 of Pathak fails to teach or suggest a frequency multiplicator unit, which frequency-multiplies the converted electrical data signal, thereby producing a frequency-multiplied signal, wherein the frequency-multiplied signal is used to drive the phase locked loop circuit, as recited in claim 1. In contrast to claim 1, column 3, lines 7-16 of Pathak merely teaches a transmit module which includes: a clock recovery circuit having an analog phase-locked loop (APLL) with multiple phase outputs. Pathak also teaches that the aforementioned transmit module may include control logic for selecting frequency multiplication ratio and output phases.

However, Pathak provides no teaching or suggestion whatsoever that the control logic for selecting frequency multiplication ratio and output phases disclosed therein produces a frequency-multiplied signal that is used to drive the analog phase-locked loop, as recited in claim 1. For example, in describing Pathak's transmit module, Pathak teaches only that the analog phase locked loop 390 receives a reference clock input REFCLK 391 and that the control and test circuitry 399 receives its inputs 393 from external pins of the ASIC chip (column 4, lines 10-40; FIG. 3). Indeed, contrary to the requirements of MPEP §2141(III)[1], the grounds of rejection fail to provide any evidence in fact and/or reasoning to support the conclusory allegations that column 3, lines 7-16 of Pathak teaches the claimed "frequency multiplicator unit." Therefore, claim 1 would not have been obvious in view of Pathak and LaGasse for *at least* these reasons.

[1] MPEP §2141(III) states that "[t]he Supreme Court in *KSR* noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit" and that "rejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."

Second, even assuming *arguendo* that column 3, lines 7-16 of Pathak *were* to teach a frequency multiplicator unit and that Pathak's clock/data recovery module 103[2] *were* to teach a clock recovery unit as alleged by the grounds of rejection (which Applicant does not concede), claim 1 nevertheless would not have been obvious in view of such teachings. Quite to the contrary, claim 1 recites a frequency multiplicator unit, which frequency-multiplies the converted electrical data signal thereby producing a frequency-multiplied signal that is used to drive the phase locked loop circuit of a clock recovery unit. In sharp contrast to claim 1, Pathak fails to provide any teaching or suggestion whatsoever that the alleged frequency multiplicator unit of column 3, lines 7-16 produces a signal used to drive a phase locked loop of the clock/data recovery module 103. In fact, Pathak clearly teaches away from such an idea.

For example, Pathak teaches that the clock/data recovery module 103 comprises prior art which the purported invention of Pathak is designed to overcome. To this effect, Pathak teaches that the clock/data recovery module 103 is one of multiple discrete high power dissipation clock recovery circuits, in a common prior art repeater module, that carry out clock recovery in a bit-stream by bit-stream basis (*see* column 1, line 48 – column 2, line 22; FIG. 1). However, the purported invention of Pathak is a transmit module wherein "[a] single high performance analog phase locked-loop circuit is used to simultaneously provide clock/data recovery for multiple bit streams" (column 3, lines 1-3; *see also* Abstract). Accordingly, Pathak teaches that by using the purportedly inventive transmit module of column 3, lines 7-16, rather than the prior art multiple high power dissipation clock recovery circuits, such as clock/data recovery module 103, the

[2] The grounds of rejection rely on Pathak's clock/data recovery module 103 as allegedly corresponding to the claimed clock recovery unit.

power dissipation required to perform clock recovery is thereby reduced to a fraction of that required in conventional transmit systems (*see* Abstract).

Thus, there would have been no reason for one of ordinary skill in the art to use the purportedly inventive transmit module of column 3, lines 7-16 of Pathak together with the prior art clock/data recovery module 103, as alleged by the grounds of rejection. Indeed, such a modification would negate Pathak's purported contribution to the art (i.e., reducing the power dissipation required to perform clock recovery to a fraction of that required using conventional multiple high power dissipation clock recovery circuits). Therefore, one of ordinary skill in the art, following the guidance found in Pathak, would be led in a direction divergent from the path that was taken by the Applicant in claim 1. Here, the Examiner relies on impermissible hindsight analysis and it is well-settled that the Examiner cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention[3]. As such, claim 1 is patentable over the cited references for *at least* these reasons.

Third, Pathak fails to teach or suggest the features of wherein the receiver device comprises a frequency filter for the spectral power of the electrical data signal, as claimed. The grounds of rejection allege that the 1:4 demultiplexer filtering in Pathak corresponds to the claimed frequency filter for the spectral power of the electrical data sign. Applicant respectfully disagrees and submits that it is technically impossible to "separate" from a 2.4 Gb/s data stream a 622 MHz clock by spectral filtering. Moreover, the 622 MHz clock 510 is used as reference input 337 to the ASIC, which performs S/P conversion and outputs a subrate clock signal at 77.75 MHz. This is used as input 391 to PLL 390, which outputs a multiplied clock signal at 622

[3] *See* In re Fine, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

MHz, again. In sharp contrast, exemplary embodiments of the claimed invention would extract a spectral component of the 2.4 Gb/s signal at, perhaps, 622 MHz, which would then be multiplied to drive a PLL that outputs a clock signal at 2.4 GHz. As such, the claimed invention is completely different than Pathak.

Fourth, the grounds of rejection have not properly considered both the invention recited in claim 1, and the cited Pathak reference, as a whole, as required by MPEP § 2141.02. When claim 1 is properly considered as a whole, there is no teaching in either the cited references, or in the knowledge generally available to one of ordinary skill in the art, of the desirability of making the specific combination that was made by the applicant as recited in claim 1. For instance, we claim 1 is properly considered as a whole, one of ordinary skill in the art would recognize that illustrative embodiments of the claimed invention are directed to recovering a clock signal from a distorted optical signal with an improved tolerance for dispersion. Along these lines, the specification explains that when transmitting high bit rate optical signals in optical fibers over long distances, such transmitted optical signals are subject to dispersion and such dispersion effects reduce the optical power within the transmitted optical signal and, consequently, it is difficult to recover a clock signal.

In contrast, when properly considering Pathak reference as a whole, one of ordinary skill in the art would easily recognize that Pathak bears no relevance at all to the invention recited in claim 1 since Pathak does not relate in any way to the question of how a clock signal is recovered from a distorted optical signal.[4] Indeed, the claimed invention relates to a receiver

[4] *See e.g.,* column 1, lines 62-63, "[t]his requires phase lock loop techniques beyond the scope of this description" (emphasis added).

side whereas, conversely, Pathak relates to the transmit side of a regenerator. Pathak's clock recovery circuit already receives a reference clock signal, while the claimed circuit receives at its input a spectral component of an O/E converted optical signal. Hence, consistent with the claimed invention, the clock generator is not driven by an external clock signal but by the spectral signal component. Moreover, Pathak explicitly says that his invention is not concerned with how the clock signal is extracted from the received optical signal (column 1, lines 59-63).

Fifth, the reasoning applied by the grounds of rejection is internally inconsistent and unsupported. For instance, Pathak discloses a clock generator unit 398, which comprises an APLL 390 that is driven by a reference clock 391. However, the grounds of rejection state that Pathak does not disclose a clock recovery unit that comprises a PLL (03/19/09 Office Action, page 5). Applicant respectfully submits that the Examiner's position in this regard is unreasonable and merely an erroneous attempt to distort Pathak's teachings so as to read Pathak's APLL 390 on the claimed frequency multiplicator unit. One of ordinary skill in the art would have recognized that, of course, a PLL can generate, from an input clock signal, a multiplied clock signal. But, this is not what the claimed invention is concerned with. Quite to the contrary, the claimed invention drives a PLL with an O/E converted data signal filtered at $1/n$ of the bitrate and multiplied by n. There is nothing in Pathak that even hints to these features.

Therefore, claim 1 is patentable over the cited references for *at least* these additional reasons. Moreover, the dependent claims 3-7 are allowable *at least* by virtue of their dependency. Thus, Applicant respectfully requests that the Examiner withdraw these rejections.

Finally, Applicant draws the Supervisory Examiner's Attention to MPEP § 707.02 and requests that the Supervisory Patent Examiner personally check on the pendency of this application with a view to finally concluding its prosecution.

VI. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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